

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.  
Serial No. : 10/069,352  
Filed : August 7, 2002

Art Unit : 2183  
Examiner : David J. Huisman  
Conf. No. : 7931

Title : FAST WRITE INSTRUCTION FOR MICRO ENGINE USED IN  
MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

**MAIL STOP RCE**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Applicant requests consideration of the references listed on the attached PTO-1449 form.  
Under 37 CFR § 1.98 (a)(2)(ii), only copies of foreign patent documents and non-patent literature are enclosed. Copies of the listed U.S. patents can be provided upon request.


This filing is being made with the filing of a Request for Continued Examination.

No fee is required. Please apply any other required fees to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date:

Feb. 22, 2007



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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-308US1	Application No. 10/069,352
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	
		Filing Date August 7, 2002	Group Art Unit 2183
(37 CFR §1.98(b))			

## U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0038403	03/2002	Wolrich et al.			
	AB	3,577,189	05/1971	Cocke et al.			
	AC	3,881,173	04/1975	Larsen et al.			
	AD	4,454,595	06/1984	Cage			
	AE	4,471,426	09/1984	McDonough			
	AF	4,477,872	10/1984	Losq et al.			
	AG	4,569,016	02/1986	Hao et al.			
	AH	4,742,451	05/1988	Bruckert et al.			
	AI	4,755,966	07/1988	Lee et al.			
	AJ	4,808,988	02/1989	Burke et al.			
	AK	4,816,913	03/1989	Harney et al.			
	AL	4,847,755	07/1989	Morrison et al.			
	AM	4,868,735	09/1989	Moller et al.			
	AN	5,045,995	09/1991	Levinthal et al.			
	AO	5,056,015	10/1991	Baldwin et al.			
	AP	5,165,025	11/1992	Lass			
	AQ	5,170,484	12/1992	Grondalski			
	AR	5,187,800	02/1993	Sutherland			
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	AT	5,202,972	04/1993	Gusefski et al.			
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	AZ	5,463,746	10/1995	Brodnax et al.			
	BA	5,509,130	04/1996	Trauben et al.			

Examiner Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	BB	5,541,920	07/1996	Angle et al.			
	BC	5,544,337	08/1996	Beard et al.			
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	BE	5,600,848	02/1997	Sproull et al.			
	BF	5,610,864	03/1997	Manning			
	BG	5,640,538	06/1997	Dyer et al.			
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	BI	5,680,564	10/1997	Divivier et al.			
	BJ	5,701,435	12/1997	Chi			
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	BL	5,748,950	05/1998	White et al.			
	BM	5,802,373	09/1998	Yates et al.			
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	BX	5,875,470	02/1999	Dreibelbis et al.			
	BY	5,898,866	04/1999	Atkins et al.			
	BZ	5,923,872	07/1999	Chrysos et al.			
	CA	5,926,646	07/1999	Pickett et al.			
	CB	5,928,358	07/1999	Takayama et al.			

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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	CD	5,943,491	08/1999	Sutherland et al.			
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	CF	5,946,222	08/1999	Redford			
	CG	5,956,514	09/1999	Wen et al.			
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	CJ	6,061,710	05/2000	Eickemeyer et al.			
	CK	6,061,711	05/2000	Song et al.			
	CL	6,101,599	08/2000	Wright et al.			
	CM	6,115,777	09/2000	Zahir et al.			
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	CO	6,141,348	10/2000	Muntz			
	CP	6,157,988	12/2000	Dowling			
	CQ	6,195,739	02/2001	Wright et al.			
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	CS	6,223,208	04/2001	Kiefer et al.			
	CT	6,223,277	04/2001	Karguth			
	CU	6,230,119	05/2001	Mitchell			
	CV	6,230,230	05/2001	Joy et al.			
	CW	6,230,261	05/2001	Henry et al.			
	CX	6,259,699	07/2001	Opalka et al.			
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	DA	6,314,510	11/2001	Saulsbury et al.			
	DB	6,338,133	01/2002	Schroter			
	DC	6,378,124	04/2002	Bates et al.			

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	DF	6,401,155	06/2002	Saville et al.			
	DG	6,408,325	06/2002	Shaylor			
	DH	6,496,847	12/2002	Bugnon et al.			
	DI	6,505,229	01/2003	Turner et al.			
	DJ	6,523,108	02/2003	James et al.			
	DK	6,543,049	04/2003	Bates et al.			
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	DM	6,560,671	05/2003	Samra et al.			
	DN	6,564,316	05/2003	Perets et al.			
	DO	6,574,702	06/2003	Khanha et al.			
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	DQ	6,976,095	12/2005	Wolrich et al.			
	DR	6,983,350	01/2006	Adiletta et al.			
	DS	7,020,871	03/2006	Bernstein et al.			

## Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	DT	0 130 381	01/1985	Europe				
	DU	0 463 855	01/1992	Europe				
	DV	0 476 628	03/1992	Europe				
	DW	0 696 772	02/1996	Europe				
	DX	WO03/019399	03/2003	WIPO				
	DY	WO03/085517	10/2003	WIPO				

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**Other Documents (Include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	DZ	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
	EA	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: <a href="http://www.romilly.co.uk/whathart.htm">http://www.romilly.co.uk/whathart.htm</a> >
	EB	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", <i>IEEE</i> , pp. 57-62, (1996).
	EC	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufmann Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
	ED	Hearing et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
	EE	Hearing et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
	EF	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
	EG	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM &amp; IEEE-CS</i> , 20(2):136-145, May 1992.
	EH	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).
	EI	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , <i>IEEE</i> , pp. 26-31 (1996).
	EJ	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	EK	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	EL	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
	EM	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).
	EN	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
	EO	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27th Annual Hawaiian International Conference on System Sciences</i> , <i>IEEE</i> , pp. 584-593, (1994).
	EP	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	EQ	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
	ER	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.

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Other Documents (include Author, Title, Date, and Place of Publication)		
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	ES	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
	ET	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

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